4–1 INTRODUCTION

4–2 A basic block diagram of the 8013B is shown in Figure 4–1 and this diagram should be referred to when reading the following description. The pulse repetition rate is generated either internally by the rate generator, manually using a push-button, or externally by an applied signal. The pulses produced can be gated synchronously by applying an external gating signal to the gate input. The output of the rate generator is fed to the selector circuits and to the trigger amplifier to produce a trigger output.

4–3 The 8013B can be used in one of three modes of operation; Normal mode, RZ mode and External Width mode. In Normal mode the pulses are generated as described above; In RZ mode external signals, applied directly to the delay generator, determine the repetition rate of the output pulses; In External Width mode external signals, applied to the Normal/Complement circuit, determine the width and repetition rate of the output pulses. The mode switching is accomplished by the selector circuits.

4–4 The output of the selector circuits, in Normal and RZ modes is applied to the delay generator which delays the pulses by the amount set on the delay controls.

4–5 In double pulse mode two pulses are produced for each trigger pulse; the normal delayed pulse plus an extra pulse that by-passes the delay generator and is thus not delayed.

4–6 The pulse spikes from the delay generator are applied to the width generator where pulses of defined width are created.

4–7 The output of the width generator or, in External Width mode, the external input signal is applied to a pulse shaper where two complementary signals are generated. These two signals are then applied to the normal/complement circuit.

4–8 The signals are then applied to two variable gain output amplifiers and attenuators. Finally the variable DC offset is added.

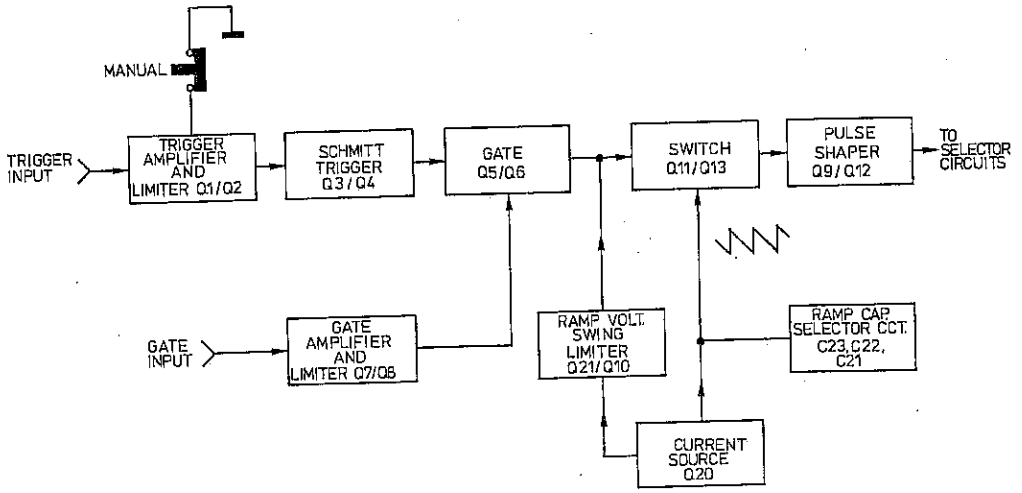

Figure 4–2. Repetition rate generator – block diagram

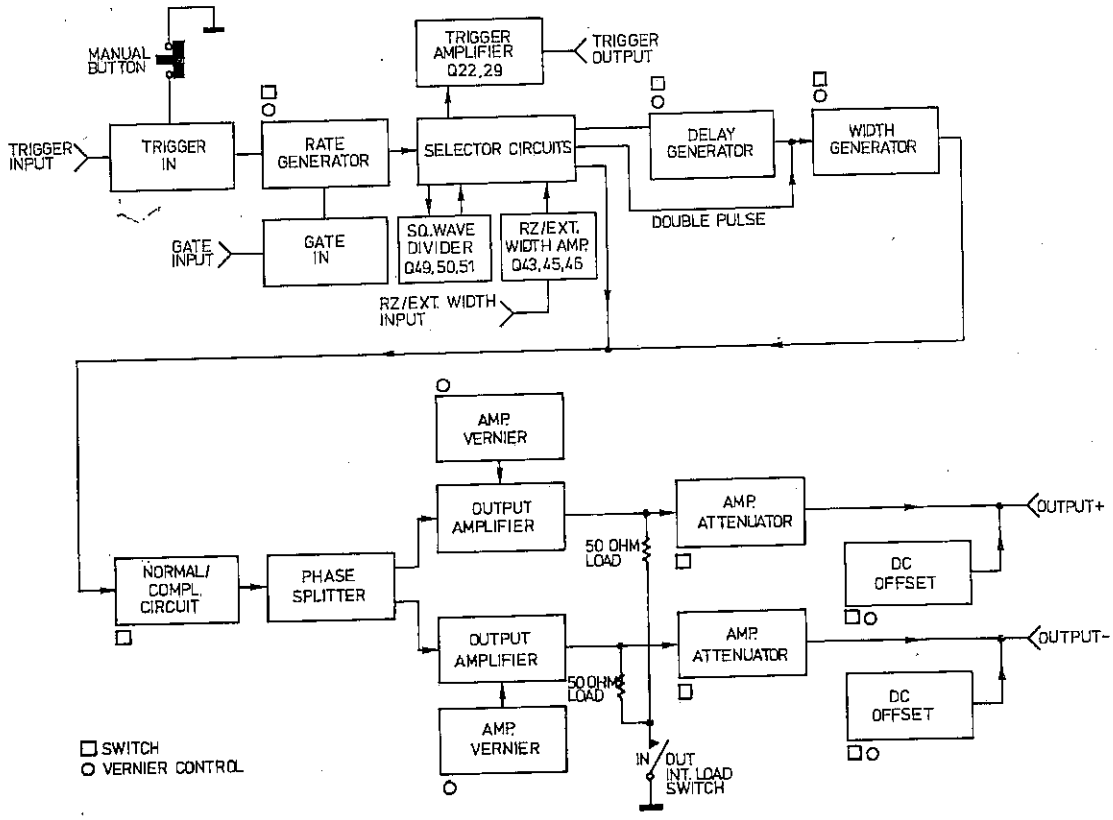

Figure 4–1. 8013B Pulse Generator — Block Diagram

4–9 REPETITION RATE GENERATOR

4–10 A block diagram of the repetition rate generator is given in figure 4–2 and a full schematic in diagram 1. These diagrams should be referred to when reading the following description.

4–11 The pulse repetition rate is determined;

a. by the internal rate generator
b. externally using an applied signal
c. manually suing a pushbutton.

4–12 Internal Rate Generator

4–13 When the internal rate generator is used, one of four period ranges is selected using the period range switch. In the three slower ranges, ramp capacitors (C23, C22, C21) are selected to provide the required repetition rate, transistors Q17, Q18 and Q19 switch these capacitors in or out. In the fastest range, no ramp capacitor is switched in; the time is determined by preset capacitor C24. In operation the selected capacitor discharges through constant current sink Q20 controlled by the pulse period vernier R1 and the value of the capacitor.

As the voltage at Q20 collector approaches zero, CR17 becomes forward biassed causing Q11 and Q13 to conduct and rapidly recharge the capacitor. The pulse period vernier controls Q21 and Q10 which act as a voltage swing limiter and determine the upper voltage limit to which the ramp capacitor can recharge. When the capacitor has recharged to this limit, Q13 and Q11 cut off thus allowing the discharge cycle to resume. The output from Q11 is applied, via the differentiator network Q28/L3/R35, to the delay generator and the trigger output amplifier.

4–14 External Trigger Operation

4–15 In external trigger mode the rate generator is used as a pulse shaper. Trigger pulses are applied to the differential amplifier Q1/Q2 which in turn switches the Schmitt trigger formed by Q3/Q4. The negative output spikes from the collector of Q4 turn Q5 on and Q13 base rises so that Q13 and Q11 turn on to produce an output pulse.

4–16 Manual Operation

4–17 When the Manual pushbutton is pressed, a negative spike is produced at the collector of Q4 which enables the current switch Q11/Q13. One pulse is produced from Q11 each time the Manual pushbutton is pressed.

4–18 GATING

4–19 Gate signals are applied to the gate amplifier Q8/Q7. Q8, normally 'off' is turned on by the 0V level (off time) of the gate input pulse. Thus Q6 is turned on, the current through Q6 lowers the base voltage of Q13 and so disables the rate generator. When the level of the gate input pulse reaches +1.8V (on time) Q8 turns on and enables the pulse source. Thus output pulses will be produced from the rate generator only during the gate input pulse 'on' time.

4–20 SELECTOR CIRCUITS

4–21 A block diagram of the selector circuits is given in figure 4–3 and is repeated for each mode of operation showing the signal paths used. Figure 4–1, 4–3 and the schematic diagram 2 should be referred to when reading the following description.

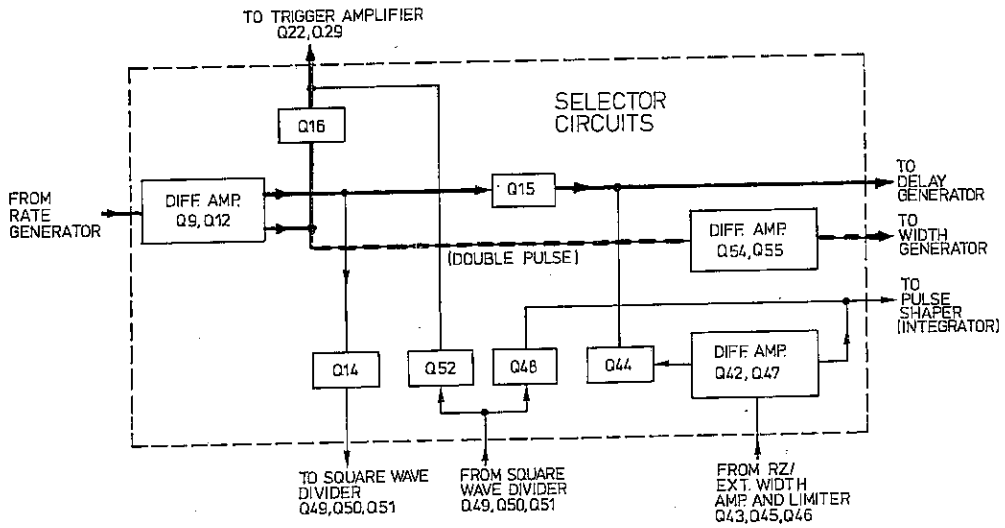

Figure 4–3a. Normal mode (including external trigger and rate mode).

4–22 In Normal mode, the rate generator output is applied to the delay generator via Q15 and to the trigger amplifier via Q16. If double pulse mode is selected, the pulse is also applied to the width generator via differential amplifier Q54/Q55 (see schematic 3).

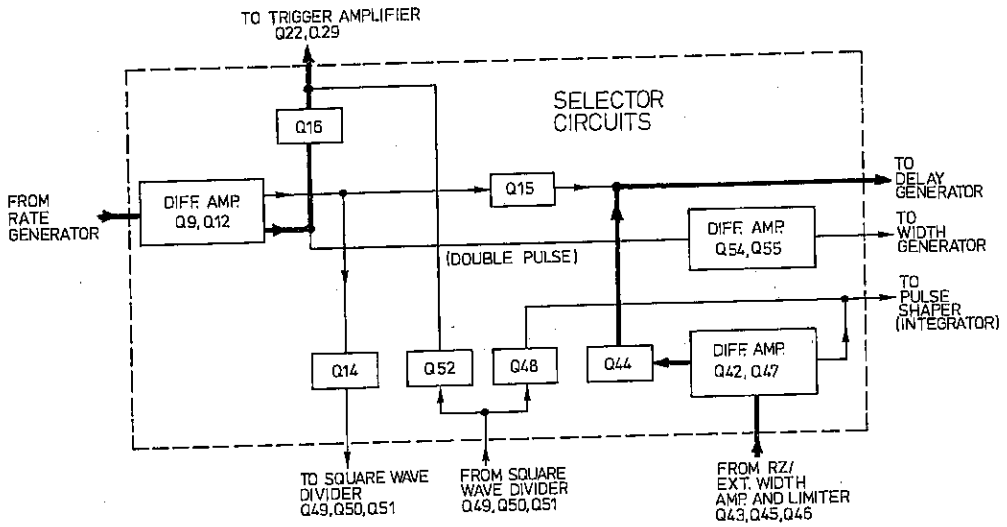

Figure 4–3b. RZ mode

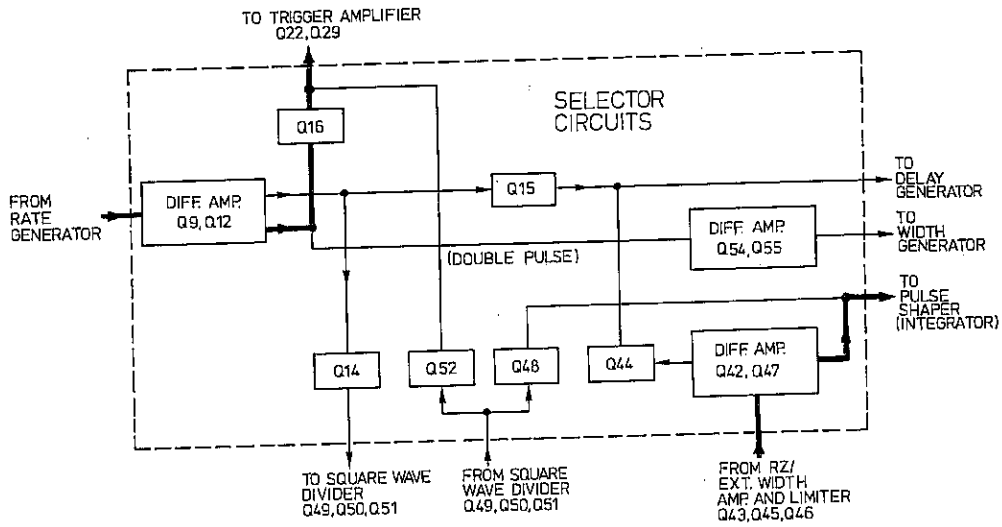

Figure 4–3c. Ext. Width mode

4–23 In RZ mode the rate generator output is only used to generate trigger pulses, via Q16. The RZ input is applied, via Q43, Q46, Q45 to the differential amplifier Q42/Q47 and gate Q44, to the delay generator.

4–24 In Ext. Width mode the rate generator output is only used to generate trigger pulses, via Q16. The Ext. Width input is applied, via Q43, Q46, Q45 to the differential amplifier Q42/Q47 to pulse shaper 3 and the integrator.

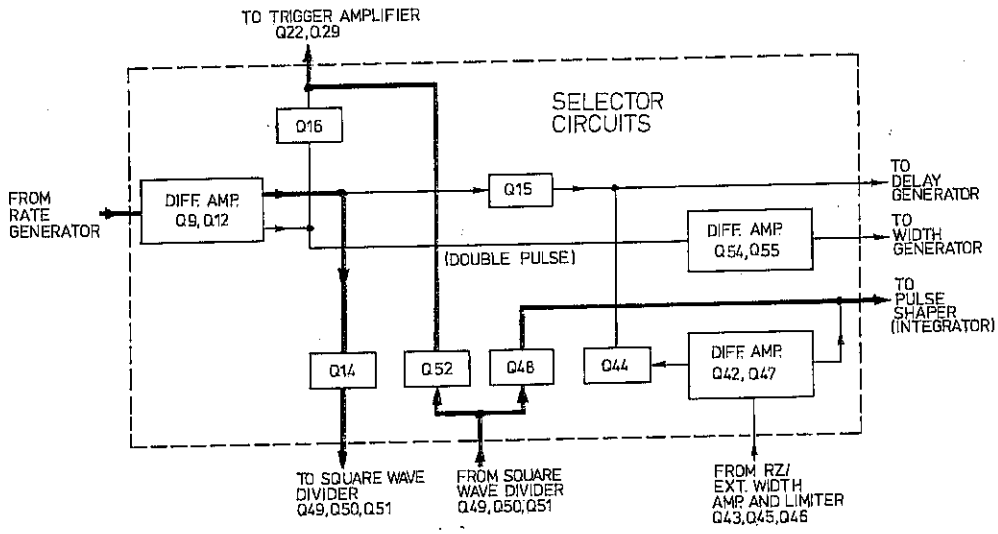

Figure 4–3d. Square wave mode

4–25 In Square wave mode the output of the rate generator is applied, via Q14, to the square wave divider. The output of the divider is applied to the trigger amplifier, via Q52, and pulse shaper 3 and the integrator, via Q48.

4–26 DELAY GENERATOR

4–27 A block diagram of the delay generator is given in figure 4–4 and a full schematic in diagram 3. These diagrams should be referred to when reading the following description.

4–28 The purpose of the delay generator is to delay the pulse source, whether from the internal rate generator, external trigger or from the RZ input, within the range of 35ns to 1s, with respect to the trigger output.

4–29 The current source (Q23), the monostable (Q30/Q31) and the recharge circuit (Q26) are controlled by the width switch so that the delay circuit is inhibited in square wave and external width modes.

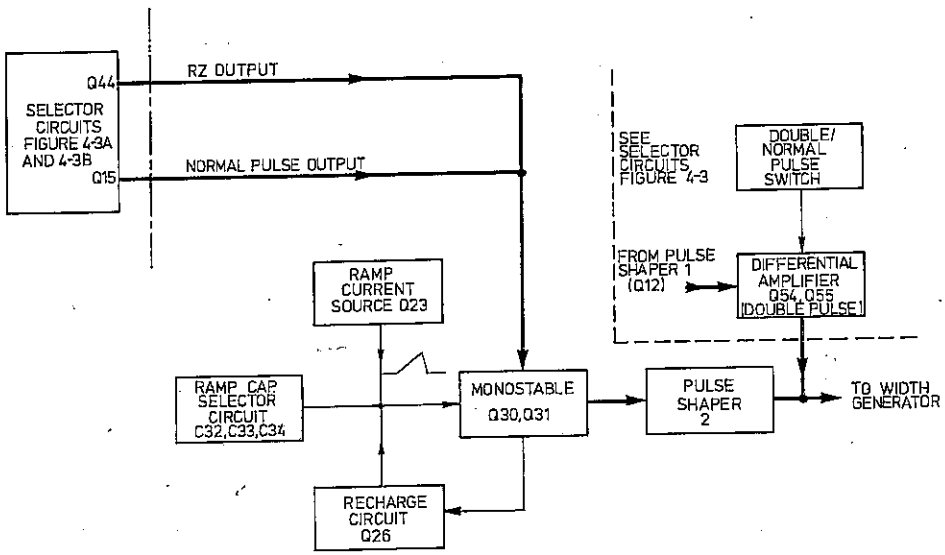

Figure 4–4. Delay generator – block diagram

4–30 Under no-signal conditions, Q31 is off, Q30 is on and Q26 is acting as a sink for the ramp current. Thus the ramp current souce (Q23) cannot charge the ramp capacitors. A positive pulse input signal turns Q31 on and Q30 off, Q26 follows Q30 collector and thus is non-conducting. The selected ramp capacitor is charged by the current source Q23 until a level is reached when Q30 turns on again, which turns Q31 off. Q26 now conducts again and rapidly discharges the selected ramp capacitor. The output from the monostable is a negative spike, coincident with the pulse input, followed by a positive spike which occurs some time later and is used to drive pulse shaper 2. The time between the pairs of spikes is the time taken for the ramp waveform to reach the threshold level of the monostable (Q30/Q31), i.e. the delay time.

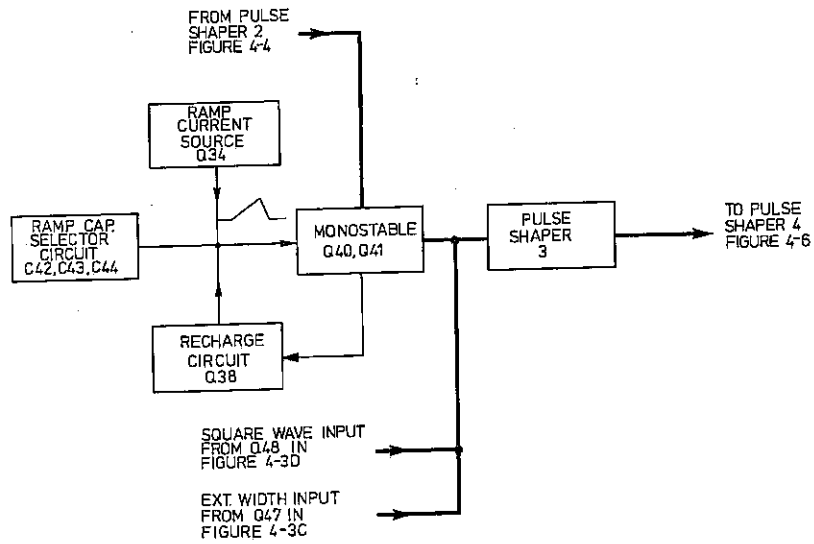

Figure 4–5. Width generator – block diagram

4–31 WIDTH GENERATOR

4–32 A block diagram of the width generator is given in figure 4–5 and a full schematic in diagram 4. These diagrams should be referred to when reading the following description.

4–33 The function of the width generator is to create a pulse of defined width for each positive pulse spike received from the delay generator. The current source (Q34) and the monostable (Q40/Q41) are controlled by the width switch so that the width circuit is inhibited in square wave and external width modes.

4–34 The width generator circuit is identical to the delay generator circuit except for the differentiator on the output (L11); see para. 4–30. The output pulse is applied to pulse shaper 3.

4–35 If square wave or external width modes are being used, the output signals from the selector circuits in figures 4–3c and 4–3d are applied directly to pulse shaper 3 and both the delay and width generators are disabled.

4–36 The two complementary outputs from pulse shaper 3 are then applied to the Normal/Complement circuit.

4–37 OUTPUT AMPLIFIERS

4–38 A block diagram of the output amplifiers is given in figure 4–6 and a full schematic in diagram 5. These diagrams should be referred to when reading the following description.

4–39 The Normal/Complement circuit consists of transistors Q29 to Q32 which are controlled in pairs

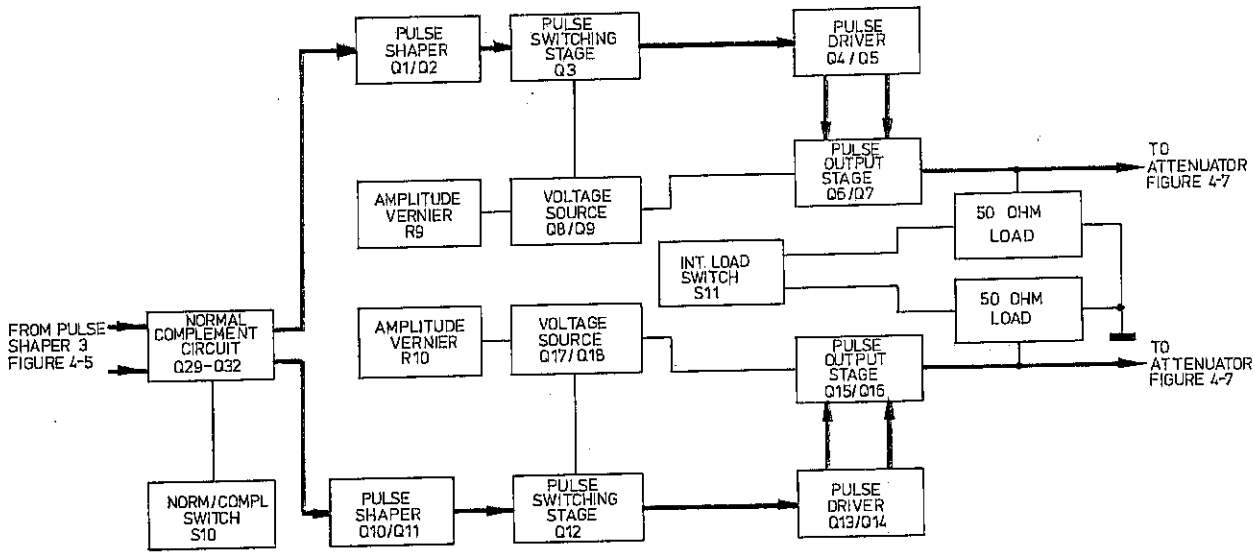

Figure 4–6. Output amplifiers – block diagram

(Q29/Q30 and Q31/Q32) by the NORM/COMPL switch (S10). Either one pair or the other is enabled to transpose the two pulse inputs.

4–40 The two complementary differentiated outputs are applied to pulse shaper Q1/Q2 for the positive channel and pulse shaper Q10/Q11 for the negative channel. The output of Q2 drives the positive output amplifier (Q4 to Q7) via a switching transistor Q3; the output of Q11 drives the negative output amplifier (Q13 to Q16) via a switching transistor Q12.

4–41 Amplitude verniers R9 and R10 determine the potential across the respective voltage sources (Q8/Q9 for the positive channel and Q17/Q18 for the negative channel). This determines the pulse amplitude swing for each channel.

4–42 When the internal load switch S11 is set to the 'in' position, relays K1 and K2 are energized and connect the 50 ohm loads to their repsective outputs.

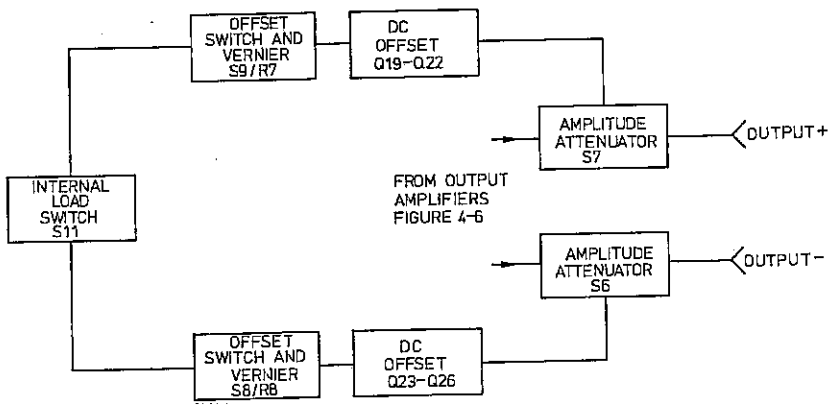

Figure 4–7. Offsets and attenuators – block diagram

4–43 OFFSETS AND ATTENUATORS

4–44 A block diagram of the offsets and attenuators is given in figure 4–7 and a full schematic in diagram 6. These diagrams should be referred to when reading the following description.

4–45 The pulses from the output amplifiers are applied to the two attenuator networks which can reduce the amplitude of each channel from 10V to 0.4V with the 50 ohm load switched out or from 5V to 0.2V with the 50 ohm load switched in.

4–46 The dc offset circuits comprise Q19 to Q22 for the positive channel and Q23 to Q26 for the negative channel. Both circuits operate in the same way and thus only the positive channel is described. Note that the offset is not available when the internal load is switched out.

4–47 When the offset switch (S9) is set to 'off', the vernier (R7) is shorted out. Thus Q19/Q20 and Q21/Q22 are switched off and deliver no current. When the offset switch is set to 'on', clockwise rotation of the vernier increases the output from Q20 and decreases the output from Q22. The output of the amplifier will then be positive. Counterclockwise rotation of the vernier causes the reverse to happen and the amplifier output to become negative.

4–48 POWER SUPPLIES

4–49 The +17V and −17V power supplies are identical series regulated types using IC regulators (U1 and U2) and series pass transistors (Q27 and Q28). Resistors R100 and R104 act as current sensing resistors to enable the regulators to limit the current output.